REMARKS

Claims 20-32 and 34-36 are pending in the application.

Claims 20-32 and 34-36 have been rejected.

Claims 1-3, and 33 have been canceled herein.

Claims 4-19 were previously canceled.

Claims 20, 23, 28, 32, and 34 are amended herein.

Claims 20-32 and 34-36 remain pending in the application.

Reconsideration of the claims is respectfully requested.

I. CLAIM REJECTIONS - 35 U.S.C. § 112

Claims 20, 23, 32 and 34 were rejected under 35 U.S.C. § 112, first paragraph as claiming subject matter that is not described in the specification in a manner enabling one skilled in the relevant art to make or use the claimed invention. This rejection is respectfully traversed.

Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. MPEP § 2164.01, p. 2100-193 (8th ed., rev. 4, October 2005). The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation.

Id. A patent need not teach, and preferably omits, what is well known in the art. *Id.* The Patent Office has the initial burden of establishing a reasonable basis to question the enablement provided for the claimed invention. MPEP § 2164.04 at 2100-197. The minimal requirement for a proper enablement rejection is to give reasons for the uncertainty of the enablement. *Id.*

The Examiner has rejected Claims 20, 23, 32, and 34 on the basis of the phrase "device that is configured to select between the configuration vector and the test vector." This element is fully supported by the specification, including paragraphs [0013], [0020], and [0021]. The use of a multiplexer to select a configuration vector is called out in paragraph [0013], as shown below:

> Thus, according to a broad aspect of the invention, a circuit is presented that includes scan chain elements to contain a vector for selective application to circuit elements of the circuit. A vector memory contains a configuration vector which, when applied to the circuit elements, configures the circuit elements into a state in which a leakage current is reduced. A multiplexer selects the configuration vector for loading into the scan chain elements, and a clock generator clocks the configuration vector into the scan chain elements. In one embodiment, a sleep mode detector is provided to configure the multiplexer to select the configuration vector and to operate the clock generator to clock the configuration vector into the scan chain elements when a sleep mode of the circuit is detected. [Emphasis Added]

The use of a multiplexer to select a test vector is called out in paragraph [0021], as shown below:

> In the circuit embodiment 10 shown, when a sleep or standby mode signal occurs, the scan-chain 12 is enabled by a LLE (low leakage enable) signal 28 in place of the normal TE signal. This is implemented by a simple multiplexer 30, which receives the TI signal 20 on one input and the LLE signal 29 on another. The selection

> signal for the multiplexers 34 and 30, as well as the LLE signal 29, is controlled by a finite state machine (FSM) 36. [Emphasis Added]

TI signal 20 is the "TI (test-in) input to which a test vector is applied in test mode" (Para. [0020], specification as filed. Therefore a multiplexer, or group of multiplexers, are disclosed to configure accept and select between "the configuration vector and the test vector" as claimed. This element is fully supported by the specification, as filed.

Claims 23 and 32 were rejected under 35 U.S.C. § 112, second paragraph for insufficient antecedent basis. These claims have been amended to overcome this rejection.

Claims 20, 23, 32, and 32 were rejected as requiring clarification of "circuit elements" and "selective application". These elements are defined throughout the specification, including paragraph [0013] which is reproduced below:

> Thus, according to a broad aspect of the invention, a circuit is presented that includes scan chain elements to contain a vector for selective application to circuit elements of the circuit. A vector memory contains a configuration vector which, when applied to the circuit elements, configures the circuit elements into a state in which a leakage current is reduced. A multiplexer selects the configuration vector for loading into the scan chain elements, and a clock generator clocks the configuration vector into the scan chain elements. In one embodiment, a sleep mode detector is provided to configure the multiplexer to select the configuration vector and to operate the clock generator to clock the configuration vector into the scan chain elements when a sleep mode of the circuit is detected.

Accordingly, the Applicant respectfully requests the Examiner to withdraw the § 112 rejection.

II. CLAIM REJECTIONS - 35 U.S.C. § 102

Claims 20-32 and 34 - 36 were rejected under 35 U.S.C. § 102(a) as being anticipated by Publication Paper "Leakage Current Reduction in Sequential Circuits by Modifying the Scan Chains, fourth international symposium on 24-28 March 2003," to *Abdollahi et al.*, hereinafter "Abdollahi". This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-76 (8th ed., rev. 4, October 2005) (*citing In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *Id.* (*citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)).

The Applicant directs the Examiner's attention to independent Claim 20, which recites unique and novel elements, including those emphasized below:

> A circuit, comprising:
> circuit elements;
> scan chain elements to contain a vector for selective application to said circuit elements;
> a vector memory for containing a configuration vector which, when applied to said circuit elements, configures said circuit elements into a state in which a leakage current is reduced;
> a multiplexer to select said configuration vector for loading into said scan chain elements wherein said first multiplexer is controlled by a finite state machine, and wherein the finite state machine comprises sleep, standby and at least one other mode;

a clock generator to clock said configuration vector into said scan chain elements;
a circuit for receiving a test vector for clocking into said scan chain elements;
wherein said multiplexer is configured to select between said configuration vector and said test vector for loading into said scan chain elements; and
wherein said clock generator is configured to clock said selected vector into said scan elements.

Applicant respectfully submits that the element "wherein said first multiplexer is controlled by a finite state machine, and wherein the finite state machine comprises sleep, standby and at least one other mode" is not anticipated by the prior art of record. Therefore, Claim 20 is patentable over the prior art of record.

Claims 23, 32, and 34 each comprise an element substantuallu simialar to the one discussed above. Claims 22, 24-31, and 35-36, depend directly or indirectly from Claims 23, 32, and 34 and are therefore similarly patentable.

Accordingly, the Applicant respectfully requests the Examiner to withdraw the § 102 rejection with respect to these claims.

CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Munck Carter Deposit Account No. 50-0208.

Respectfully submitted,

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